IDEC Chip Design Contest

A 10b Source-Driver IC with LSB-Stacked LV-to-HV-Amplify DAC Achieving 2688μm²/channel and 4.8mV DVO for Mobile OLED Displays

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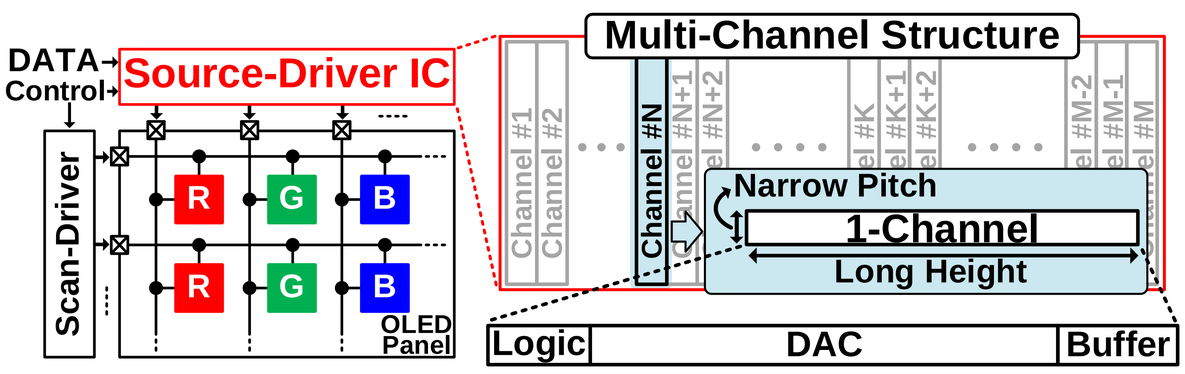
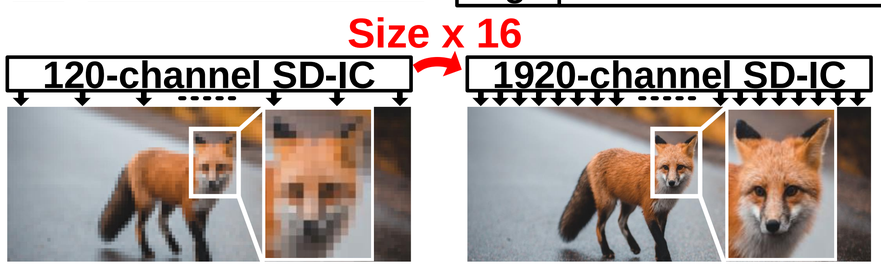
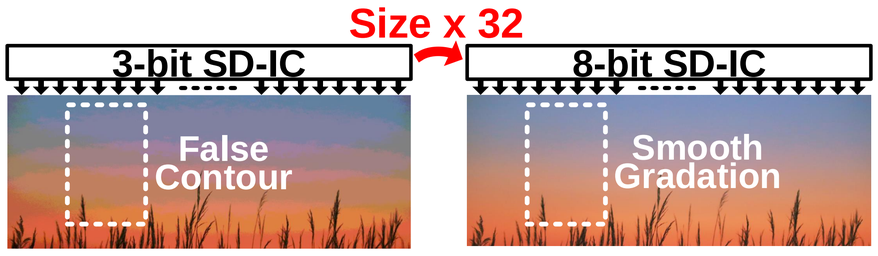
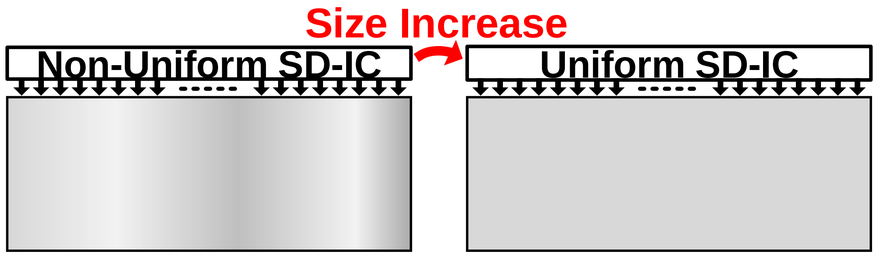
Abstract

- This paper presents a display source-driver IC with LSB-stacked LV-to-HV-amplify 10b DAC.
- The mismatch-insensitive x4-multiplier enables an 8b R-DAC to be realized with LV compact TRs while outputting the high voltages.
- The proposed LSB stack-up scheme consuming little area extends the DAC resolution to 10b.



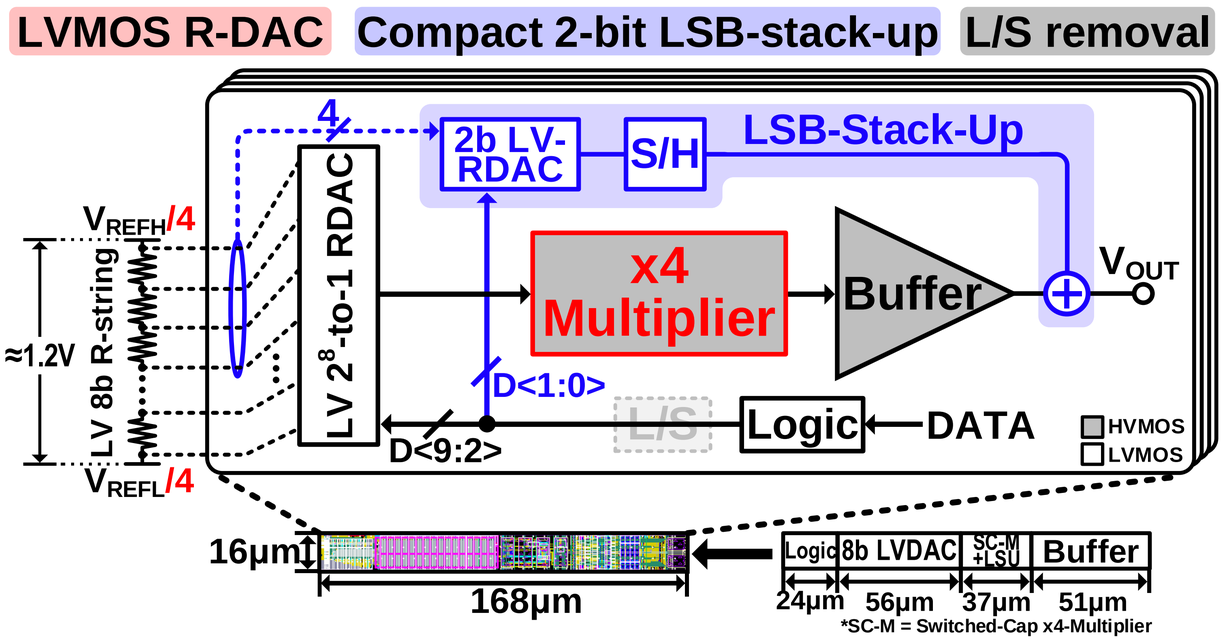






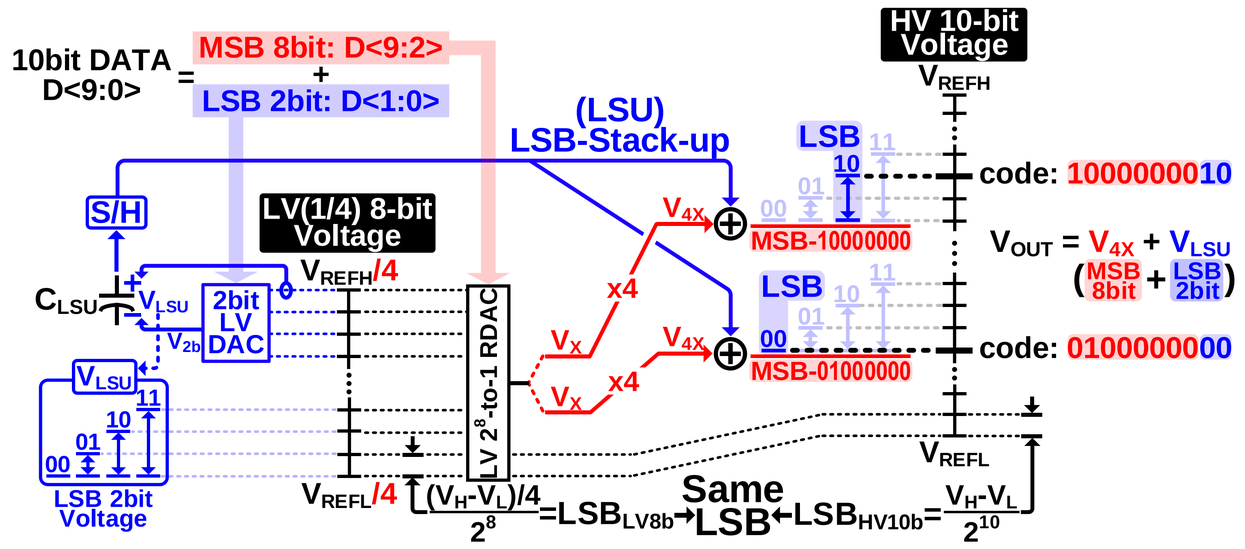
Motivation

- Source-Driver IC (SD-IC) has a multi-channel structure
- Since size of SD-IC is increases proportional to every importa nt performance metrics, it has a trade-off relationship with othe r performance metrics
- SD-IC with compact size & good performance is required



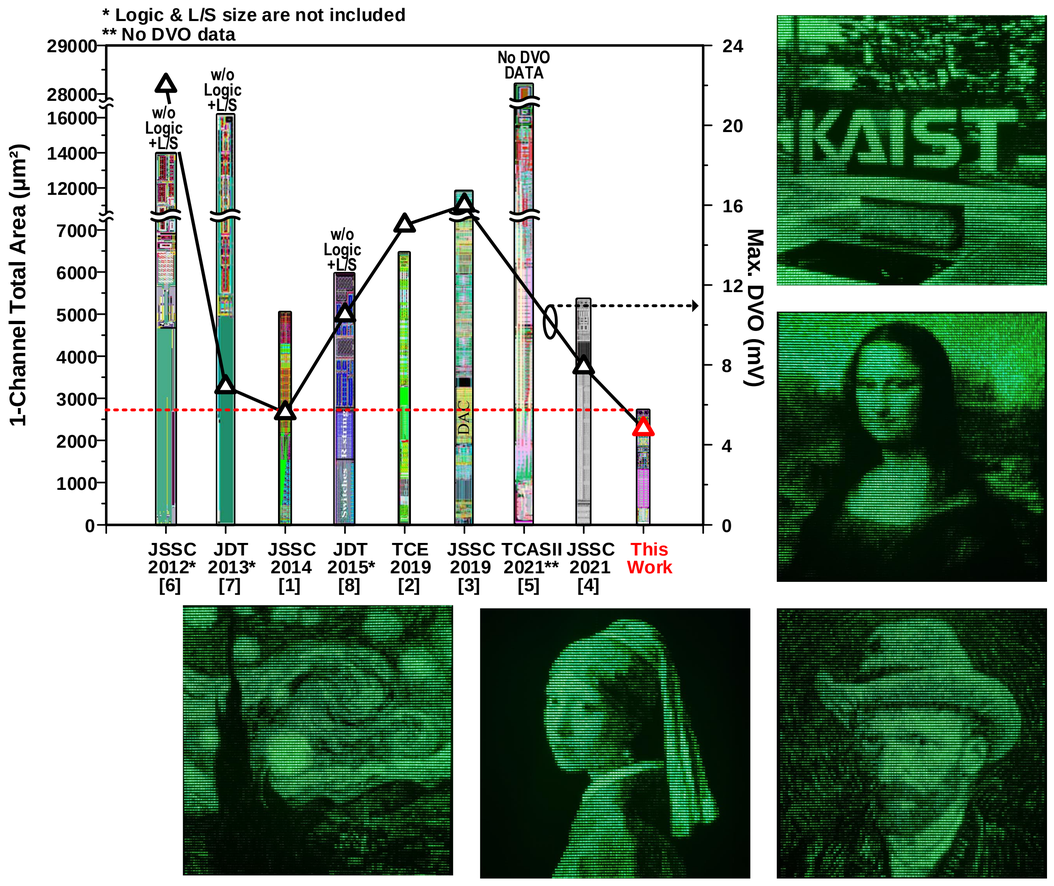
Proposed Structure & Size Reduction Technique

- R-DAC is composed of compact LVMOS instead of HVMOS
- LSB-stack-up technique extends the resolution from 8b to 10b
- Level-shifter is removed due to use of LVMOS R-DAC



Proposed LSB-Stack-Up Technique

- 10b HV output is generated from 8b LV reference.
- 8b MSB is generated by amplifying LV reference by 4-folds
- 2b LSB is generated by S/H and stack-up the 2b LSB voltages.



	JSSC'14 [1]	IEEE TCE'19 [2]	JSSC'19 [3]	JSSC'21 [6]	**This Work**
Technology	110nm CMOS	100nm CMOS	180nm CMOS	90nm CMOS	**130nm CMOS**
Gray Scale	10-bit	10-bit	10-bit	10-bit	**10-bit**
Output Range	0.25 V to 4.75 V	0.25 V to 4.75 V	0.2 V to 17.8 V	0.2 V to 4.8 V	**0.3 V to 4.5 V**
DNL / INL	0.25 / 0.43 LSB	0.4 / 0.7 LSB	0.14* / 0.46* LSB	0.2 / 0.42 LSB	**0.39 / 0.9 LSB**
Current / Channel	0.9 μA	1 μA	7 μA	2.8 μA	**1.8 μA**
Max. DVO	5.6 mV	15 mV	16 mV	7.9 mV	**4.82 mV**
1-Channel Area	5010 μm² (334 x 15)	6440 μm² (460 x 14)	11730 μm² (510 x 23)	5328 μm² (296 x 18)	**2688 μm² (168 x 16)**
Area Shrinkage**	15.4%	10.7%	N/A	31.0%	**65.2%**
Area Ratio***	186%	239%	436%	198%	**100%**

***Simulated results **Compared to conventional 8b RDAC, of which layout was individually done by each reference paper. ***100% x (1-channel total area of each reference paper / 1-channel total area of this work)**

Measurement Results

- Proposed DAC achieved smallest size and best uniformity.
- 100 x 100 mini-LED display demonstration is also performed

Conclusion

- This work, which is capable of driving HV (0.3 to 4.5V), achieves the smallest size (168×16μm² per channel) and the best DVO (4 .82mV) performance among 10b SD-ICs.
- The 1-channel area of the presented chip is approximately 2 to 4× smaller than those of other chips.